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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/723,348	11/27/2000	Jean-Francois Link	00-RO-266	5977

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EXAMINER	
DINH, MINH	

ART UNIT	PAPER NUMBER
2132	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/723,348	Applicant(s) LINK ET AL.	
	Examiner Minh Dinh	Art Unit 2132	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 November 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This action is in response to the amendment filed 02/02/2005. Claims 1-4, 6, 8-9, 11, 13, 20-22, 25-26, 28, 30, 32-33 and 36 have been amended. The abstract has also been amended.

2. Applicant states that claim 14 has been amended and the status identifier of the claim also shows "Currently Amended"; however, the claim has not been amended. Correction is required.

3. Claims 22 and 30 have been amended; however, the status identifiers of the claims show "Original". Correction is required.

4. The objection to claim 14 in the previous Office Action has not been addressed in the amendment. Applicant is reminded to respond to the objection in the next reply.

Response to Arguments

5. Applicant's arguments with respect to claims 1 and 20 have been considered but are not persuasive. Applicant's amendments have necessitated a new search and new grounds of rejection.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-8, 16-27, 32 and 35-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Milios et al. (5,860,099).

Regarding claim 1, which is exemplary of claim 20, Milios discloses a device comprising: memory protection logic operable to prevent direct readout of protected data in memory, wherein access to said protected data is restricted for access by a local processor for execution within the device (col. 1, lines 14-21; col. 2, lines 4-20; col. 3, lines 50-62); validation logic, operative in a first mode, for checking the validity of said data and for producing a validity signal to determine whether said data is valid, the validity signal being a checksum value (col. 4, lines 1-26; col. 5, lines 37-50). Milios does not explicitly disclose validity signal output control logic for inhibiting an output of said validity signal to outside said device until the validity of a predetermined quantity of said protected data has been checked. However, this feature is deemed to be inherent to the Milios device as lines 7-14 of column 4 and lines 37-40 of column 6 show that the validity signal is not output until after all of the memory is checked. The Milios device

would be inoperative if there were no validity signal output control logic for inhibiting the output of the validity signal until the validity of the memory has been checked.

Claims 2-8, 21-27 and 32 are rejected on the same basis as claims 1 and 20.

Regarding claims 16, 19 and 36, Milios further discloses that the device is implemented in a microcontroller unit (col. 1, lines 14-34; col. 3, lines 51-62).

Regarding claim 17, Milios further discloses that the memory means is a read-only memory (col. 3, lines 27-29).

Regarding claims 18 and 35, Milios further discloses that the protected data comprises program code (co. 6, lines 55-56).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 9-10, 12, 14-15, 28-29, 31 and 33-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Milios as applied to claim 1 above, and further in view of Noll (6,185,696).

Regarding claims 9 and 28, Milios does not disclose that the device comprises a device reset function for resetting the checking means in response to a device reset in the first mode. Noll discloses reset means for resetting checking means in response to

a system reset which meets the limitation of a device reset (col. 1, lines 34-41; col. 4, lines 11-23; col. 6, lines 6-10). It would have been obvious to one of ordinary skill in the art at the time the invention was made modify the Milios device such that the device comprises a device reset function for resetting the checking means in response to a device reset, as taught by Noll. The motivation for doing so would have been to prevent possible system malfunctions upon system resets due to errors in the BIOS ROM.

Regarding claims 10 and 29, Milios does not disclose that the device comprises means for exiting from the first mode upon a device reset. Noll discloses means for exiting from the first mode upon a system reset which meets the limitation of a device reset (col. 1, lines 34-41; col. 4, lines 11-23). It would have been obvious to one of ordinary skill in the art at the time the invention was made modify the Milios device such that the device comprises reset means for resetting the checking means in response to a device reset, as taught by Noll. The motivation for doing so would have been to prevent possible system malfunctions upon system resets due to errors in the BIOS ROM.

Regarding claims 12 and 31, Milios does not disclose reset means operative to reset the validity signal upon the device being force to leave the first mode prematurely. Noll discloses reset means operative to reset the validity signal upon a system reset (col. 1, lines 34-41; col. 4, lines 11-21). It would have been obvious to one of ordinary skill in the art at the time the invention was made modify the Milios device such that the device comprises reset means operative to reset the validity signal upon a system reset, as taught by Noll; the system reset forces the device to leave the first mode

prematurely. The motivation for doing so would have been to prevent possible system malfunctions at system resets due to errors in the BIOS ROM.

Regarding claims 14 and 33, Milios does not disclose that the memory means comprises a chip enable input, the input being connected to selection means for delivering an enable signal when a first mode selection signal and a protection option signal are active. Noll discloses that the memory means comprises a chip enable input, the input being connected to selection means for delivering an enable signal when a first mode selection signal a protection option signal are active (col. 3, lines 29-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made modify the Milios device such that the memory means comprises a chip enable input, the input being connected to selection means for delivering an enable signal when a first mode selection signal and a protection option signal are active, as taught by Noll. The motivation for doing so would have been to selectively enable and disable the primary BIOS ROM and the secondary BIOS ROM.

Regarding claims 15 and 34, Milios further discloses that an address belonging to the memory means is selected at an address input in order to enable the memory means (col. 4, lines 9-11).

10. Claims 11 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Milios in view of Noll as applied to claims 10 and 29 above, and further in view of Jablon et al. (5,421,006). Noll discloses a device reset function (col. 1, lines 34-41; col. 4, lines 11-23; col. 6, lines 6-10). However, Milios and Noll do not disclose that the

device reset function comprises latching means for temporarily latching a logic state indicating the presence of the first mode and gating means for transferring the device reset signal to a reset input of the validation logic only when said logic state is present in the latching means, the latching means temporarily maintaining said gating means enabled after a caused by the device disappearance of the reset signal logic state. Jablon discloses a device for assessing the integrity of computer system software which includes reset means; the reset means comprising latching means and gating means (Abstract and fig. 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made modify the device of Milios and Noll such that the device reset function comprises latching means and gating means, as taught by Jablon; accordingly, the latching means if for temporarily latching a logic state indicative of the presence of said first mode, and the gating means is for controllably passing said device reset signal to a reset input of said checking means when said logic state is latched. The motivation for doing so would have been to protect the codes in the non-volatile memory from being overwritten by subsequent untrusted programs.

11. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Milios as applied to claim 1 above, and further in view of Tanenbaum ("Structured Computer Organization"). Milios does not disclose explicitly that the validity signal output control logic is implemented in hardware. Tanenbaum teaches that hardware and software are logically equivalent and that any operation performed by software can also be built directly into hardware (page 10, "A central theme of this book ... make different

decisions."). It is obvious to one of ordinary skill in the art at the time the invention was made that the Milios validity signal output control logic can be implemented in hardware, as taught by Tanenbaum. The decision to put certain functions in the hardware could be made according to the system requirements.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Dinh whose telephone number is 571-272-3802. The examiner can normally be reached on Mon-Fri: 10:00am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gilberto Barron can be reached on 571-272-3799. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MD

Minh Dinh
Examiner
Art Unit 2132

MD
4/29/05

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